corresponding six-bit input word.

+1 → 0

Detailed Description Text - DETX (16):

It will be appreciated that when the levels are plus or minus one, the magnitude of the input word is already zero. Accordingly, the third step is also the last and no string of zeros representing magnitude is generated. It will be noted that for level plus one there is a single zero in the variable length output word. However, this zero represents polarity. The polarity-representing bit always appears as the second bit of the variable length output word and is therefore generated in the second step.

Detailed Description Text - DETX (31):

In addition to OR gate 76, sign bit detection means 42 comprises a flip-flop 78 having its output connected to one input of OR gate 76. Its CLk input is connected to the Q output of flip-flop 64 and its D input is connected to the Q output of flip-flop 50 in the input means 30. The sign or polarity bit is the second bit of the variable length word so when the low to high transition (at the time of the second bit) appears at the CLK input of the sign bit flip-flop 78, it will latch whatever bit is then appearing at the input, which is the second bit of the variable length word at the Q output of flip-flop 50. This polarity bit is then transferred by way of OR gate 76 to the adder 40 for

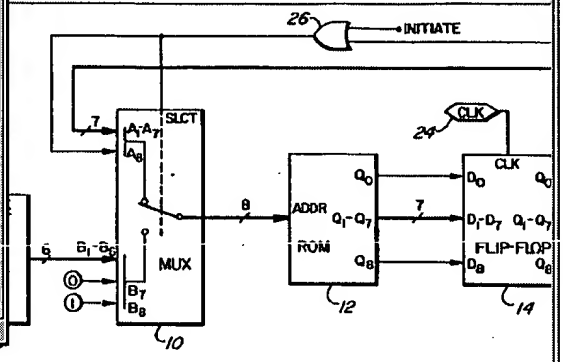

FIG. 1

	U	1	Document ID	Issue Date	
15			US 4215415 A	19800729	Recursiv and feedl detecting
16			US 4580129 A	19860401	Variable
17			EP 222942 A1	19870527	Variable

Brief Summary Text - BSTX (13):

FIG. 1 provides a variable length code table for the CCITT recommendation H.261. The table encodes each of 127 fixed length code words as a corresponding unique VLCW. Each fixed length code word is a pair of a run and a level. The level may be a positive or a negative value. The variable length code associated with each fixed length code word has a sign bit "s" for indicating whether the level has a positive polarity (i.e., s=0) or a negative polarity (i.e., s=1).

Detailed Description Text - DETX (17):

Unlike the conventional VLD design, which uses separate VLD tables for positive and negative polarities of each VLCW, in the present invention, the VLD table decodes, the positive and negative polarities of each VLCW the same way, i.e., into an absolute value of the fixed length code word. This reduces the storage requirement of the variable length decoding table by half. In addition, the variable length decoding table, according to the invention, decodes slightly shorter VLCWs, i.e., which are one bit shorter by virtue of not decoding the sign bit.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
18			US 4568916 A	19860204	Variable
19			US 5663725 A	19970902	VLC dec
20			US 4646327 A	19870224	Waveforr

FIG. 2
(PRIOR ART)

		STH	CODE-WORD	NO.	LEVEL	CODE
			10	34	14	0000 0000 1001 1s
			1s	35	6	0011 0s
				35	11	0000 0011 11s
			11s	36	13	0000 0001 0010 s
				37	7	0001 11s
			0100 s	48	11	0000 0010 01s
			0010 1s	49	7	0001 01s
			0000 110s	40	13	0000 0001 1110 s
			0010 0110 s	41	7	0001 00s
			0010 0001 s	42	13	0000 0001 0101 s
			0000 0010 10s	43	8	0000 111s
			0000 0001 1101 s	44	13	0000 0001 0001 s
			0000 0001 1000 s	45	8	0000 101s
			0000 0001 0011 s	46	14	0000 0000 1000 1s
			0000 0001 0000 s	47	9	0010 0111 s
			0000 0000 1101 0s	58	14	0000 0000 1000 0s
			0000 0000 1100 1s	59	9	0010 0011 s
			0000 0000 1100 0s	50	9	0010 0010 s
			0000 0000 1011 1s	51	9	0010 0000 s
			011s	52	11	0000 0011 10s
			0001 10s	53	11	0000 0011 01s
20	9		0010 0101 s	54	11	0000 0011 00s
21	11		0000 0011 00s	55	13	0000 0001 1111 s
22	13		0000 0001 1011 s	56	13	0000 0001 1010 s
23	14		0000 0000 1011 0s	57	13	0000 0001 1001 s
24	14		0000 0000 1010 1s	68	13	0000 0001 0111 s
25	5		0101 s	69	13	0000 0001 0110 s
26	8		0000 100s	60	14	0000 0000 1111 1s
27	11		0000 0010 11s	61	14	0000 0000 1111 0s
28	13		0000 0001 0100 s	62	14	0000 0000 1110 1s
29	14		0000 0000 1010 0s	63	14	0000 0000 1110 0s
30	6		0011 1s	64	14	0000 0000 1101 1s
31	9		0010 0100 s	65	6	0000 01
32	13		0000 0001 1100 s			

Detailed Description Text - DETX (5):

Referring to FIG. 2, multiplier 1 is a digital multipler includes an input register 36 which is connected to data input line 34. The input register 36 is connected to a 2's complement generator 38 which simultaneously provides the 2's complement of each data byte stored in the input register 36 to AND gate arrays 40 and 42, respectively. The n bits of the output of 2's complement generator 38 are provided to a set of parallel AND gates which are all combined with the most significant bit of the sine and cosine coefficients, respectively. The 2's complement of each data input signal is used for this purpose in order to properly maintain the word length of the data input signals which ma change in polarity from plus to minus. The outputs of AND gate arrays 40 and 42, respectively, are provided to adders 44 and 46, respectively, which add the input data signal multiplied by the most significant bit of the cosine and sine coefficients, respectively to an n-bit ground signal. The sum of these two numbers is stored in storage registers 48 and 50, respectively. These signals, along with the data input signal, are provided to the next multiplier stage.

and cosine function generators
sets of m-bit digital coefficients.
type circuit of claim 6 wherein
rage means comprises a plurality
each bit of said digital sine and

co-sine coefficients, wherein each shift register includes a number of stages corresponding to the ranking in significance of each bit of said coefficients.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
3			DE 2514529 A	19761021	Digital ph spacing b by specia
4			US 4791600 A	19881213	Digital pip
5			US 3650842 A	19720321	ELECTR

the logic circuit 156 shown in FIG. 1. The output signal of the buffer 231 is applied to a run-length decoder 232 which decodes the position of the polarity changes, disables AND gate 217, and enables AND gate 234. In accordance with the manner in which the polarity information is coded, either one of these two AND gates, 217 and 234, supplies signals to OR gate 223. A polarity detector 224 connected to the output of OR gate 223 decodes the two polarity code words and correspondingly either sets or resets the polarity memory 226 which controls the polarity switch 221. The polarity detector 224 supplies an output signal which informs the run-length decoder 232 of changes in polarity. When the absolute magnitude code words emerge from the delay 216, they are applied to the converter 218 which produces the analog equivalents of the coded quantized signal. For the run-length coded sign changes, the polarity memory 226 is controlled by a polarity code word that corresponds to the run-length code word location of the buffer 231 made available to the polarity memory 226 by enabling AND gate 234. The result is that switch 121, controlled by the polarity memory 226, provides the polarity change between the two successive absolute magnitude code words which had exceeded the predetermined level in the transmitter 111 of FIG. 1. From the output of switch 221, the run-length coded sign changes are accumulated in accumulator 222 in the same manner as any other received information. The output of accumulator 222 is a reconstructed replica of the input analog signal to the transmitter 111 of FIG. 1 obtained from the video input source 112.

	U	1	Document ID	Issue Date	
1	☐	☑	US 4028535 A	19770607	Apparatu null
2	☐	☐	US 3689840 A	19720905	CODING
3			DE 2514529 A	19761021	Digital ph spacing b

is invention is a run-length
it which supply coded infor-
the location of sign changes
two successive differential
both exceed a predetermined
mission during the horizontal

ures of the invention will
ading the detailed description
companying drawing.

N OF THE DRAWINGS

m of a transmitter embodying
on; and
m of a receiver for decoding
tted from the transmitter of

DESCRIPTION

am of a transmitter 111 em-
f the present invention. An
for example, a video input
low pass filter 113 and sam-
although the input signal is a
understood that the applica-
ot restricted to video signals
may be transmitted by the in-
of the sampler 114 is applied
subtracts the output signal of
ferred to as the prediction
to obtain a differential signal.
gnal of the subtractor 116 is
of an analog-to-digital con-
on, converter 119, quantizes
magnitude of the differential
ion, converter 121, codes the
mple.
mple has the same sign as the
ple, the absolute magnitude
put of the converter 119 is
th for the output of the con-
verter 119 through the transmitter 111 comprises AND gate 122, OR gate 123, a delay 124, AND gate 126, OR gate 127, and AND gate 128 which is enabled by a horizontal drive signal to allow transmission of the output signal through OR gate 129. This is the path of the output signal of transmitter 111 which is used most frequently and which is used between sign changes of the differentially sampled video analog input signal. The transmission of the absolute magnitude code words by the transmitter 111 is made possible by a low level output signal of a polarity change detector 137 to which is applied the output signal of the converter 121. In the absence of a change in sign between differential samples, the output signal from the polarity change detector 137 disables AND gates 139 and 141, which in turn respectively enable AND gates 123 and 126 to allow transmission of the absolute magnitude signals through the previously described path.

The absolute magnitude code words from OR gate 123 are also applied to a first section, sign and absolute magnitude decoder 132, of a digital-to-analog converter 131 in a feedback path used to provide the prediction signal. The analog output signal of the decoder 132 is applied to an amplifier 134 through a subtractor 133. The amplifier 134 has a positive and a negative output signal both of which are applied to a switch 136. The converter 121 controls the position of the switch 136 such that the polarity of the output signal from the amplifier 134 applied to the accumulator 117 is the same as the polarity of each differential sample applied to the converter 121. The accumulator 117 provides the prediction signal which was previously mentioned in connection with the operation of the subtractor 116.

The output signal of the polarity change detector 137 goes to a high level which can enable AND gates 138, 139 and 141 upon the occurrence of a change from one polarity word to the other polarity word, indicating a sign change between two successive differential samples applied to the converter 121, in the output signal of the converter 121. AND gates 138, 139, 141 and 147 provide output signals which determine whether the absolute magnitude signals are going to be transmitted and how the polarity word output from the converter 121 is going to be substituted into the absolute magnitude signals. The operation of AND gates 138, 139, 141 and 147 is controlled by the evaluation of the input and output signals of a delay 142 by comparators 143, 144 and 146. The comparator 143 compares the digitally coded absolute magnitude input signals with the output signals of the delay 142 which provides a delay equal to one sampling interval. Thus, the input and output signals are two successive signals from the converter 121. If the output signal is differential sample S_n, then the input signal will be differential sample S_{n+1}. Comparators 144 and 146, on the other hand, compare the input and output signals respectively to a predetermined level. The output signals of comparators 146 and 146 are applied to AND gate 147 which applies an output signal to AND gates 138, 139 and 141. The output signal from the comparator 143 is applied to AND gates 138 and 139 and OR gate 148 to which is also applied the output signal of AND gate 147. The output signal of OR gate 148 is applied to AND gate 141.

The operation of the circuitry set forth in the foregoing will not be considered on the basis of different signaling conditions of the differential samples that produce a change in sign between the coded differential samples. If the coded differential sample with the change in sign is smaller than that of the previous differential sample, the comparator 143 produces an output which is applied to OR gate 148 and which disables AND gate 139. At the same time, comparators 144 and 146 compare the two successive samples with a predetermined level and produce outputs that are applied to AND gate 147. If both of the successive samples do not exceed the predetermined level in comparators 144 and 146, AND gate 147 provides an output signal which disables AND gates 138 and 139 and is applied to OR gate 148. The output of OR gate 148 enables AND gate 141 to which also is applied the enabling signal of the polarity change detector 137. This causes the output of AND gate 141 to change level such that AND gate 122 which was previously enabled is now disabled and AND gate 149 which was previously disabled is now enabled. The switch between the states of AND gates 122 and 149 blocks the transmission of the absolute magnitude code word on the second successive sample and substitutes the polarity word output

EAST Browser - L32: (20) word near2 l... | US 3689840 A | Tag: S | Doc: 2/20 (SORTED) | Format: KWIC

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gates may be inhibited by the operation of the polarity change detector on the smaller of the two successive differential samples between which the change in sign occurs. The output of the first converter will not be inhibited unless both successive samples exceed the predetermined level. If the output signal from the first converter is inhibited, a polarity word indicating the new polarity from the output of the second converter is substituted for the smaller of the two successive absolute magnitude code words. If, however, both successive samples have a larger magnitude than the predetermined level, one of two polarity words followed by a run-length code word indicative of the location of the change in sign will be transmitted during the horizontal retrace interval. When the run-length code word is used, the absolute magnitude of both of the two successive code words is transmitted. The run-length coding and interrupting of the transmission of the first converter are controlled by a gating network to which is applied the output signals of the first, second and third comparator circuits and the polarity change detector.

Detailed Description Text - DETX (9):

If the two successive samples each exceed the respective predetermined levels of comparators 144 and 146, when a change in sign is detected by polarity change detector 137 and AND gate 138 is enabled, the output level of AND gate 147 changes state thereby directly enabling AND gate 138 and disabling

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
1	☐	☑	US 4028535 A	19770607	Apparatu null
2	☐	☐	US 3689840 A	19720905	CODING
3			DE 2514529 A	19761021	Digital ph spacing b

...e invention is a run-length ...it which supply coded infor... ...the location of sign changes ...two successive differential ...both exceed a predetermined ...mission during the horizontal

...tures of the invention will ...ading the detailed description ...companying drawing.

...N OF THE DRAWINGS

...m of a transmitter embodying ...m; and

...m of a receiver for decoding ...itted from the transmitter of

...DESCRIPTION

...am of a transmitter 111 em... ...f the present invention. An ..., for example, a video input ...low pass filter 113 and sam... ...although the input signal is a ...understood that the applica... ...ot restricted to video signals ...may be transmitted by the in... ...of the sampler 114 is applied ...subtracts the output signal of ...ferred to as the prediction ...to obtain a differential signal. ...gnal of the subtractor 116 is ...of an analog-to-digital con... ...on, converter 119, quantizes ...magnitude of the differential ...on, converter 121, codes the ...mple.

...mple has the same sign as the ...ple, the absolute magnitude ...put of the converter 119 is ...th for the output of the con... verter 119 through the transmitter 111 comprises AND gate 122, OR gate 123, a delay 124, AND gate 126, OR gate 127, and AND gate 128 which is enabled by a horizontal drive signal to allow transmission of the output signal through OR gate 129. This is the path of the output signal of transmitter 111 which is used most frequently and which is used between sign changes of the differentially sampled video analog input signal. The transmission of the absolute magnitude code words by the transmitter 111 is made possible by a low level output signal of a polarity change detector 137 to which is applied the output signal of the converter 121. In the absence of a change in sign between differential samples, the output signal from the polarity change detector 137 disables AND gates 139 and 141, which in turn respectively enable AND gates 123 and 126 to allow transmission of the absolute magnitude signals through the previously described path.

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------- KWIC -------

Brief Summary Text - BSTX (17):

In the above-mentioned Franaszek patent, a method is disclosed for forc binary waveform to have zero DC component by keeping the running sum contributions of each clock cycle and then choosing the next data word fro list, any member of which will cause the sum not to grow larger in the sam polarity. The methods employed here are based on the bounding of the ru sums of the Fourier components at the frequency to be suppressed. For e there is a code of word length N= 10 and run length 6 such that 256 choic bits) exist for any polarities of s.sub.2 and c.sub.2 which are desired. Thu this code has an efficiency of 80%.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
1			US 4028535 A	19770607	Apparatu null
2			US 3689840 A	19720905	CODING
3			DE 2514529 A	19761021	Digital ph spacing b

The method employed in preparing a lookup table in accordance with this invention is as follows: A list of all possible words of length N which meet the primary criteria (such as run length) is drawn up. Each word is examined, and a triple (s_r, c_r, p) is computed, as defined above. Then the list is divided into four sublists labelled ++; +−; −+; and −−. A word is placed in the ++ sublist, for example, if it has a non-negative value of s_r and of c_r. Words having zero value for s_r or c_r appear in several sublists. The shortest sublist determines the maximum number of data words which may be encoded without ambiguity such that the sums s_r and c_r remain bounded. When a word is to be encoded, the current waveform polarity (which is the same as the running sum of p modulo 2) and the running sums s_r and c_r are examined. When the polarity is positive, the sublist corresponding to the (sign of s_r), (sign of c_r) is used for encoding, if negative the sublist with both signs negated is used. If the code word is the number M, the Mth entry is used. This is a read-only-store (ROS) with a lookup table-type of encoding. A similar table is used for decoding. In general, the number M will require less than N bits for binary representation, so the efficiency of this encoding is less than one. However, the energy in the waveform at frequency f_r is zero, and the energy indicated by a detector of finite bandwidth and sampling time is also bounded.

In addition to this general case, there are several special cases of interest: a) Only codde words with $s_r = 0$, $c_r = 0$ are used. Then no running sums need be kept.

EAST Browser - L32: (20) word near2 t... | US 4028535 | Tag: S | Doc: 1/20 (SORTED) | "Full" 6/12 (Total images 12)

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——— KWIC ———

Brief Summary Text - BSTX (17):

In the above-mentioned Franaszek patent, a method is disclosed for forc binary waveform to have zero DC component by keeping the running sum contributions of each clock cycle and then choosing the next data word fro list, any member of which will cause the sum not to grow larger in the sam polarity. The methods employed here are based on the bounding of the ru sums of the Fourier components at the frequency to be suppressed. For e there is a code of word length N= 10 and run length 6 such that 256 choic bits) exist for any polarities of s.sub.2 and c.sub.2 which are desired. Thu this code has an efficiency of 80%.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
1	☐	☐	US 4028535 A	19770607	Apparatu null
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In addition to this general case, there are several special cases of interest: a) Only codde words with $s_r = 0$, $c_r = 0$ are used. Then no running sums need be kept. However, the efficiency is lower, usually about 50%. b) An external clock is available to control a synchronous

period
at the e
may be
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-1,
be
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The p
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EAST Browser - L4|: (13) lens with (c... | JP 04293006 A | Tag: S | Doc: 2/13 (SORTED) | Format: KWIC

File Edit View Tools Window Help

TITLE: CONVERSION ADAPTER DEVICE FOR INTERCHANGEABLE LENS SYSTEM

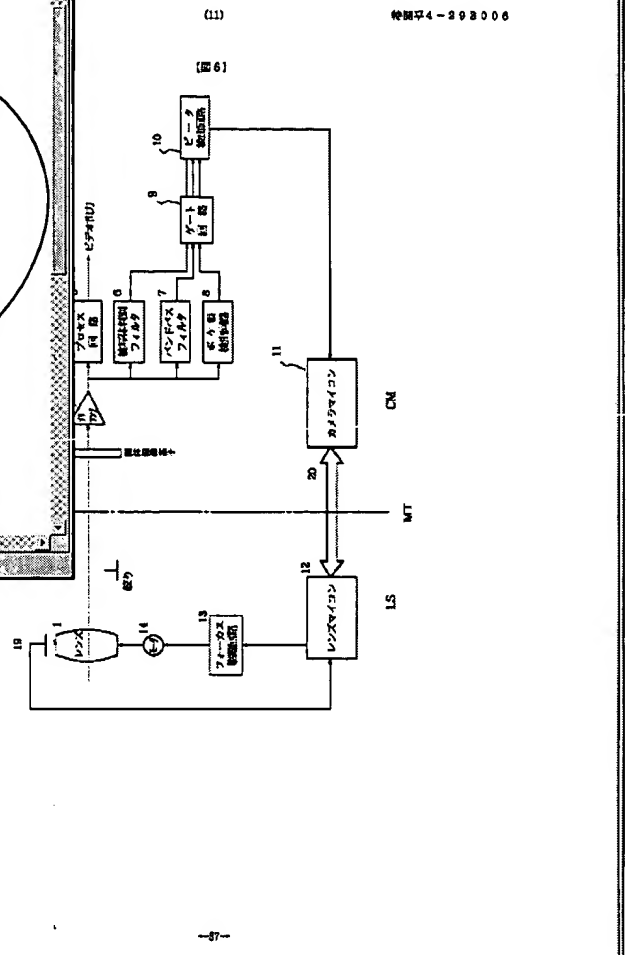
——— KWIC ———

Abstract Text - FPAR (2):

CONSTITUTION: This conversion adapter device has a focus control means 12 which performs focus detection on a camera main body side and outputs focus control information for driving a focusing lens 1 to the lens unit according to the detection result and an information converting means 15 which converts the focus control information outputted by the camera main body into a format capable of controlling the lens unit when the camera main body side and lens unit side are different in the format of the focus control information. The information converting means 15 is equipped with the compensating means 18 which compensates the lens unit according to the focal length or aperture value of the lens unit. The control speeds of lenses which have similar optical characteristics and similar tendencies in compensation quantity can be adjusted to obtain intended control speeds.

Details Text Image HTML KWIC

	U	1	Document ID	Issue Date	
1			US 6630950 B1	20031007	Apparatu
2			JP 04293006 A	19921016	CONVER LENS SY
3			US 5001566 A	19910319	Documer



EAST Browser - L24: (12) format near2... | US 6130717 A | Tag: S.TI | Doc: 4/12 (SORTED) | Format: KWIC

File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: US 6130717 A
See image for Certificate of Correction

TITLE: Image pickup apparatus with a lens unit attachment/detachment indication

——— KWIC ———

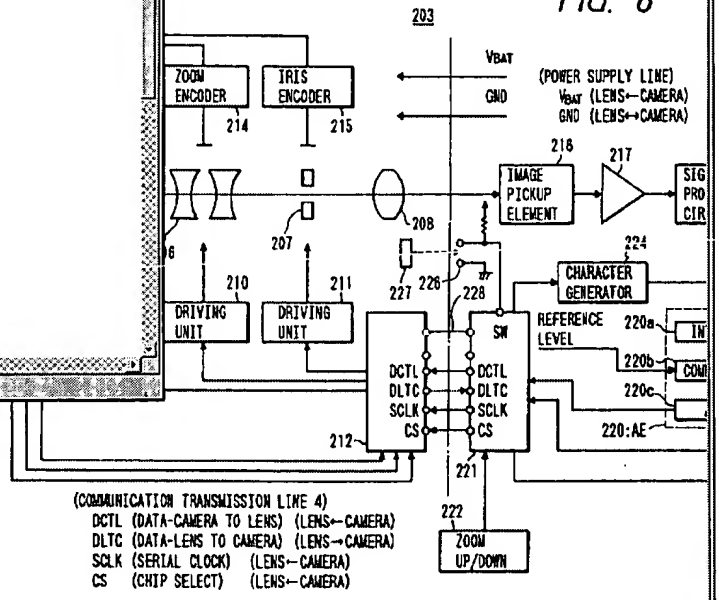
Detailed Description Text - DETX (77):

A focus state detection signal output from the AF circuit 219, an iris state detection signal output from the AE circuit 220, and an operation signal from the zoom switch 222 are fetched by the microcomputer 221. The microcomputer 221 performs predetermined arithmetic operations with reference to the operating state information sent back from the lens side. The input signals are converted into signal having a format supplied to the lens side. The converted signals are transmitted to the lens side through the communication transmission line 204, thereby controlling the lens side.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
4			US 6130717 A	20001010	Image pic indication
5			US 6392702 B1	20020521	Image pic
6			US 5600371 A	19970204	Image pic control

FIG. 8



DOCUMENT-IDENTIFIER: US 5257058 A
See image for Certificate of Correction

TITLE: Interchangeable lens system

-------- KWIC --------

Detailed Description Text - DETX (15):

A focus state detection signal from the AF circuit 305, a diaphragm state detection signal from the AE circuit 306, and an operation signal of the zoom switch 308 are supplied to the camera microcomputer 307, then subjected to predetermined processing with reference to the function state signals sent from the lens through the conversion adapter 201, further converted into a format for supply to the lens, and supplied to the conversion adapter 201 through the communication line 601. Then said signals are converted into a control data format for the still camera lens, and transmitted to the lens through the communication line 501 for effecting the lens control.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
6	☐	☐	US 5600371 A	19970204	Image pic control
7	☐	☑	US 5257058 A	19931026	Interchan
8			US 5877811 A	19990302	Interchan

US005257058A

atent [19]

[11] Patent Number: 5,257,058

[45] Date of Patent: Oct. 26, 1993

LENS SYSTEM

buchi, Tama, Japan

hiki Kaisha, Tokyo,

ication Data

00,573, Nov. 27, 1991, aban-

Priority Data

2-333836

2-333837

G03B 17/00

354/286

354/286, 289.12, 484

[56] References Cited

U.S. PATENT DOCUMENTS

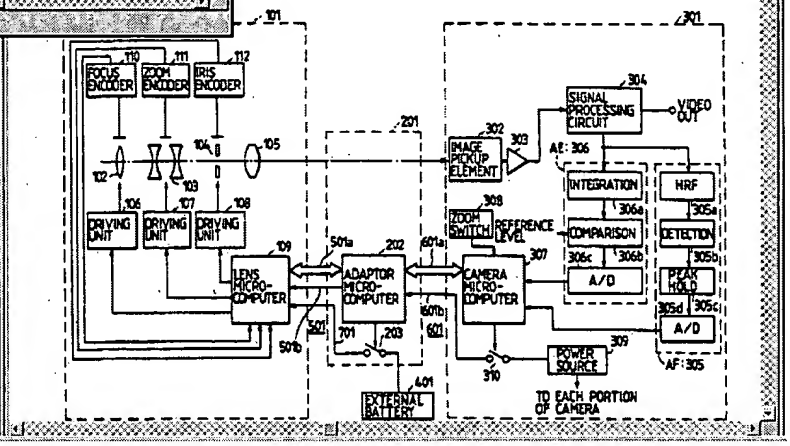
5,068,680 11/1991 Kawasaki et al. 354/286

Primary Examiner—Michael L. Gellner
Assistant Examiner—Howard B. Blankenship
Attorney, Agent, or Firm—Robin, Blecker, Daley & Driscoll

[57] ABSTRACT

An interchangeable lens system comprising a lens unit; a camera body provided with a first electric power supplying battery; a conversion adapter for connecting the camera body with the lens unit, thereby enabling electric power supply from the battery in the camera body to the lens unit; a second electric power supplying battery connected to the conversion adapter and controllable independently from the first battery; and a control circuit for enabling electric power supply from the second battery to the lens unit only when the camera body is connected to the conversion adapter.

17 Claims, 3 Drawing Sheets



EAST Browser - L23: (16) 22 and camera | JP 02267510 A | Tag: S | Doc: 2/16 (SORTED) | Format : KWIC

File Edit View Tools Window Help

TITLE: CONVERTER FOR IMAGE PICKUP MACHINE

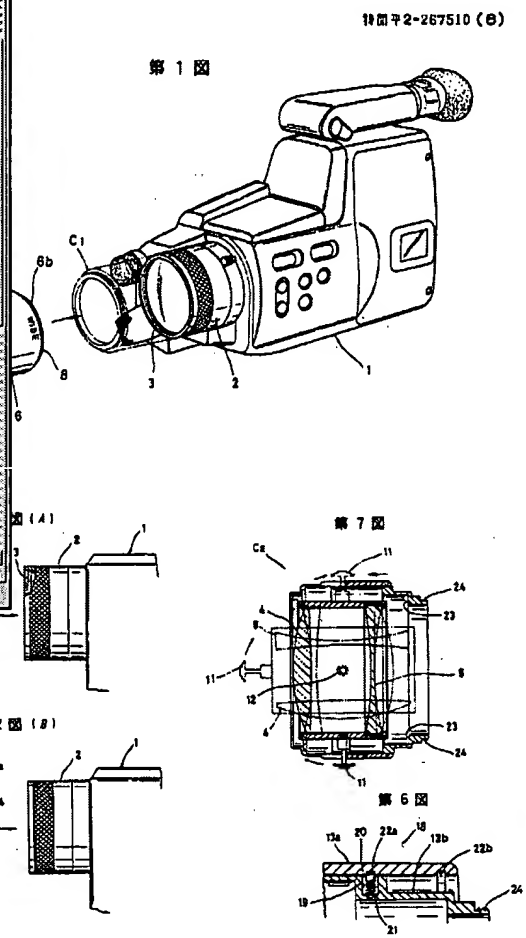
-------- KWIC --------

Abstract Text - FPAR (2):

CONSTITUTION: Lenses 4, 5 constituted of two pieces are integrated into a converter C<SB>1</SB>, and screw parts 7, 8 are formed in both end edge parts 6a, 6b of a lens holder 6. When this converter C<SB>1</SB> is installed in a lens part 2 of an image pickup machine body such as a TV camera, etc., by setting its convex lens 4 side to the outside, it works as a tele-converter and a telephoto image is obtained. On the other hand, when the converter C<SB>1</SB> is reversed, and installed by setting a concave lens 5 side to the outside, it works as a wide-converter, and a wide image is obtained. Therefore, it becomes unnecessary to carry two pieces of converters used exclusively for telephoto use and wide-angle use.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
1		P	US 5053798 A	19911001	Automatic
2			JP 02267510 A	19901101	CONVER
3			JP 63168638 A	19880712	Electronic measures



EAST Browser - L20: (104) 19 and camera | US 5434637 A | Tag: S | Doc: 22/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

TITLE: Control apparatus

-------- KWIC -------

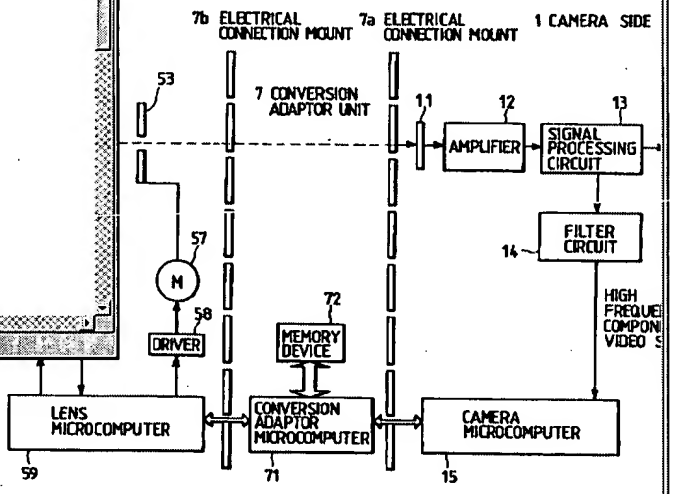
Detailed Description Text - DETX (5):

In FIG. 3, reference numeral 1 denotes the camera unit section of an exchangeable lens system of a video movie camera; 2 the lens section of an exchangeable lens system of a still camera; 7 a conversion adapter section which is used to mechanically, optically, and electrically connecting both of the camera unit section 1 and the lens section 2 and to match communication formats and the like of them. Reference numerals 7a and 7b indicate mounts which are respectively connected to the camera side and the lens side; 71 a conversion adapter microcomputer to convert and match various kinds of control information between the lens unit and the camera unit in the conversion adapter; and 72 a memory device to update the stored contents of the data which is necessary for various kinds of controls on the basis of commands which are generated from the conversion adapter microcomputer 71.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
21			US 4506958 A	19850326	Compact
22			US 5434637 A	19950718	Control a
23			JP 04293006 A	19921016	CONVER LENS SY

FIG. 3



EAST Browser - L20: (104) 19 and camera | US 5325149 A | Tag: S,T1 | Doc: 18/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: US 5325149 A
See image for Certificate of Correction

TITLE: Camera system with interchangeable lens

——— KWIC ———

Detailed Description Text - DETX (6):

In the lens unit, the diaphragm aperture value obtained from the diaphragm encoder 11 is converted by an A/D converter 25 into digital data, which are converted, together with a lens number specific to each lens, into serial control information of a predetermined format by the lens microcomputer 21, and transmitted to the camera microcomputer 20 through the communication line 22.

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
17	☐	☐	US 6608651 B2	20030819	Camera s uncontroll
18	☐	☑	US 5325149 A	19940628	Camera s
19			US 5126884 A	19920630	Compact

US005325149A

s Patent [19]

[11] Patent Number: 5,325,149

[45] Date of Patent: Jun. 28, 1994

M WITH
ABLE LENS

Kawahara, Hasogaya, Japan

Kabushiki Kaisha, Tokyo,

, 1993

. Application Data

No. 75,465, Jan. 11, 1993, which is
r. No. 818,171, Jan. 4, 1992, aban-

tion Priority Data

an 3-002243

..... G03B 7/08
..... 354/446; 354/286;
348/363
..... 354/446, 451, 452, 286;
351/225, 228

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T DOCUMENTS

..... 354/286
..... 354/286
..... 351/225

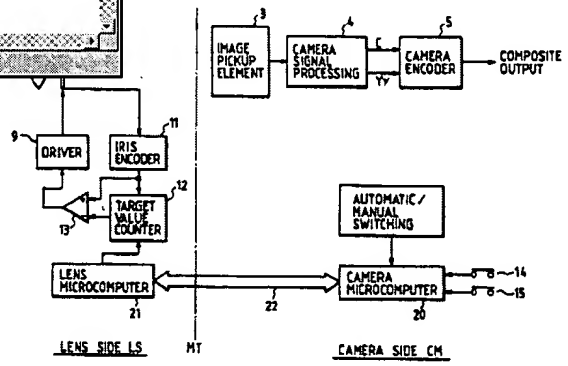
5,166,365 12/1992 Kawahara 351/228

Primary Examiner—Russell E. Adams
Attorney, Agent, or Firm—Robin, Blecker, Daley & Driscoll

[57] ABSTRACT

A camera system with interchangeable lens, consisting of a camera unit and a lens unit detachably mountable on the camera unit, comprising a target value setting circuit for setting a target control value of a diaphragm provided in the lens unit, a correction circuit for generating a correction signal for varying the content of the target value setting circuit, a diaphragm state detection circuit for detecting the diaphragm information, a first control circuit for varying the set value of the target value setting circuit, based on the correction signal, a diaphragm drive circuit for driving the diaphragm according the result of comparison of the output of the diaphragm state detection circuit and the value of the target value setting circuit, a memory circuit for storing the information specific to each lens unit, and a second control circuit for generating, at the detaching and mounting of the lens unit, a command for controlling the value of the target value setting circuit for bringing the diaphragm to a predetermined state, by referring to the content of the memory circuit.

21 Claims, 8 Drawing Sheets



EAST Browser - L20: (104) 19 and camera | US 5485208 A | Tag: S.T1 | Doc: 10/104 (SOATED) | Format: KWIC

File Edit View Tools Window Help

Detailed Description Text - DETX (13):

A focus-state detection signal which is outputted from the AF circuit 19, an iris-state detection signal which is outputted from the AE circuit 20, and operation signals which are respectively outputted from the zoom switch 22 and the AZ-mode setting switch 23 are supplied to the microcomputer 21. The microcomputer 21 then performs predetermined operations by making reference to information indicative of the various operating states transmitted from the lens assembly 1, thereby converting the supplied signals into a format suitable for transmission to the lens assembly 1. The signal thus converted is transmitted to the lens assembly 1 over the communication line 4 for the purpose of controlling the lens assembly 1.

Detailed Description Text - DETX (14):

The functions of major elements included in the lens assembly 1 and the camera assembly 2 will be described in brief hereinbelow.

Detailed Description Text - DETX (17):

In the lens assembly 1, the iris driving part 11 is driven on the basis of the control signal. Thus, the quantity of light transmitted to the camera

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
9	☐	☐	US 6654187 B2	20031125	Camera I
10	☐	☑	US 5485208 A	19960116	Camera s
11			US 5111223 A	19920505	Camera s

FIG. 1(a)

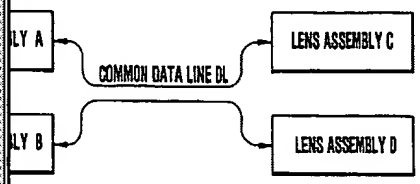
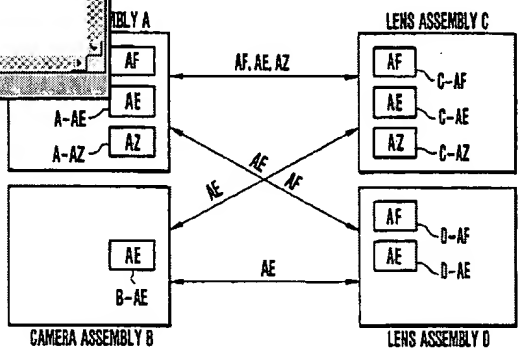


FIG. 1(b)



conversion adapter. Therefore, the still camera lens unit can be controlled as in the video camera lens unit.

Detailed Description Text - DETX (195):

As described above, for example, a still camera lens is mounted on a video camera having a format different from that of the still camera lens, the conversion means of the present invention or the conversion adapter serving as the conversion means is used to perform the same control as in mounting of the video lens unit in the video camera system such that good AF control can be performed when a still camera system interchangeable lens is connected to the video camera system of the video movie interchangeable lens system.

Claims Text - CLTX (6):

3. An interchangeable lens type camera for driving a lens unit in accordance with control data sent through an adapter being capable of mounting a lens unit which is not operable to said camera since a control format of each function of the lens unit is different from a control format of corresponding function of said camera, by adaptably converting the control format of said each function of said lens unit to the control format of said corresponding function of said camera, comprising:

	U	1	Document ID	Issue Dat	
4	☐	☐	US 5001566 A	1991031 9	Document reading apparatus
5	☐	☐	JP 04273225 A	1992092 9	INTERCHANGEABLE LENS S
6	☐	☐	US 5877811 A	1999030 2	Interchangeable lens type came

US005877811A

s Patent [19] [11] Patent Number: 5,877,811
[45] Date of Patent: Mar. 2, 1999

LE LENS TYPE CAMERA

ke Iijima, Ebina; Toshiaki i, Tama; Seiya Ohta, a, all of Japan

Kabushiki Kaisha, Tokyo,

1997

Application Data

. 238,585, May 5, 1994, abandoned, of Ser. No. 827,940, Jan. 29, 1992,

ation Priority Data

an 3-012095
an 3-012101
an 3-034763
an 3-043651
an 3-043657
an 3-092299

..... H04N 5/225
... 348/375; 348/373; 348/220; 396/71
..... 348/373, 374, 375, 315, 220, 222, 335; 396/71

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5,257,058 10/1993 Mabuchi 354/286
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1-93722 4/1989 Japan G03B 7/20

Primary Examiner—Bipin Shalwala
Attorney, Agent, or Firm—Robin, Blecker & Daley

[57] ABSTRACT

This invention discloses an interchangeable lens type video camera for deciding lens specifications on a camera side and changing control data transmitted from the camera side to a lens unit in accordance with specifications of the lens unit, thereby performing optimal control. A video camera is also disclosed in which an adapter for mounting a lens unit on the video camera is arranged, and control data outputted from the video camera side to the lens unit is corrected in accordance with lens characteristics, thereby performing the same operation as in a case wherein a video camera lens is mounted on the video camera.

28 Claims, 35 Drawing Sheets